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EXAMINER

SAVLA, ARPAN P

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PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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|------------------------------|-------------------------------|---------------------------------|--|
| Office Action Summary | Application No. 10/715,595 | Applicant(s) KUSUMOTO ET AL. | |
| | Examiner Arpan P. Savla | Art Unit 2185 | |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 31 October 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1 and 4-29 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1 and 4-29 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/ are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>10/31/07</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Amendment

This Office action is in response to Applicant's communication filed October 31, 2007 in response to the Office action dated May 31, 2007. Claims 1 and 4-29 are pending in this application.

ACKNOWLEDGMENT OF REFERENCES CITED BY APPLICANT

Information Disclosure Statement

1. As required by MPEP § 609(c), Applicant's submission of the Information Disclosure Statements dated August 21, 2007 are acknowledged by the Examiner and some of the cited references have been considered in the examination of the claims now pending. As required by MPEP § 609 c(2), a copy of the PTOL-1449 initialed and dated by the Examiner is attached to the instant Office action.
2. The Information Disclosure Statement (IDS) filed August 21, 2007 fails to comply with the provisions of 37 CFR 1.97, 1.98 and MPEP § 609 (see reasons directly below). It has been placed in the application file, but the information referred to therein has not been considered as to the merits. Applicant is advised that the date of any re-submission of any item of information contained in this IDS or the submission of any missing element(s) will be the date of submission for purposes of determining compliance with the requirements based on the time of filing the statement, including all certification requirements for statements under 37 CFR 1.97(e). See MPEP § 609.05(a).

3. References AA and AB have already been cited by the Examiner in the PTO-892 dated January 20, 2006.
4. Reference AG has not been considered by the Examiner because the reference does not comply with 37 CFR 1.98 (a)(3)(ii). The reference is a non-English-language document, however, there is no copy of an English-language translation of the document, or portion thereof.
5. Reference AH has not been considered by the Examiner because the reference does not appear to be within the file wrapper or anywhere else on the record.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. **Claims 15-17, 19-25, and 29 are rejected under 35 U.S.C. 103(a) as being obvious over Yamada et al. (U.S. Patent 5,950,222) (hereinafter "Yamada") in view of Iwata (U.S. Patent 5,881,295) and Microsoft, "Computer Dictionary, Fifth Edition" (hereafter "Computer Dictionary").**
8. **As per claim 15**, Yamada discloses a microcomputer comprising:
a nonvolatile memory including at least a first storage area and a second storage area in which delete and write of data is electrically performed independently (col. 3,

lines 12-19; Fig. 1, element 1); *It should be noted that "EEPROM" is analogous to "nonvolatile memory", "region A" is analogous to "first storage area", and "region B" is analogous to "second storage area."*

wherein a plurality of interrupt vectors indicating respective storage places of a plurality of interrupt programs executed upon requesting of an interrupt is stored in the first storage area (col. 8, lines 25-29; Fig. 8, elements (31-1)~(31-n));

and a plurality of alternate interrupt vectors corresponding to the respective interrupt vectors is stored in the second storage area (col. 8, lines 22-25; Fig. 8, elements (30-1)~(30-n));

a central processing unit that has a mechanism to access the nonvolatile memory (col. 3, lines 19-23 and 28-29; Fig. 1, element 2).

Yamada does not expressly disclose a flag indicating that the first storage area is not accessible;

and a conversion circuit that includes a first pair of registers for setting a first address range corresponding to the first storage area and a second pair of registers for setting a second address range corresponding to the second storage area, and that, when an address within the first range is accessed by the central processing unit, performs address conversion based on a state of the flag, to convert the first address range to the second address range.

Iwata discloses a flag indicating that the first storage area is not accessible (col. 9, lines 51-55 and 58-61; col. 10, lines 50-58; Fig. 1, element 18); *It should be noted that when the built-in ROM is in boot or user program mode the contents of the built-in*

ROM are not accessible. MS0 and MS1 are flags indicating whether the built-in ROM is in boot or user program mode respectively, therefore, MS0 and MS1 are also flags that indicate the built-in ROM is not accessible.

and a conversion circuit that includes a first pair of registers for setting a first address range corresponding to the first storage area and a second pair of registers for setting a second address range, and that, when an address within the first range is accessed by the central processing unit, performs address conversion based on a state of the flag, to convert the first address range to the second address range (col. 14, lines 6-15; col. 23, line 60 – col. 24, line 13; Fig. 5; Fig. 19). *It should be noted that the “vector address storage area A-V” is analogous to the “first address range”, the “vector address storage area B-V” is analogous to the “second address range”, registers “PEREG” and “MBREG1” are analogous to the “first pair of registers for setting a first address range”, and registers “PEREG” and “MBREG2” are analogous to the “second pair of registers for setting a second address range.”*

Yamada and Iwata are analogous because they are from the same field of endeavor, that being microcomputers.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Iwata's conversion circuit within Yamada's microcomputer.

The motivation for doing so would have been to improve the safety of a system during on-board programming of a program memory (Iwata, col. 3, lines 25-27). Also, another motivation for doing so would have been to provide additional safety by preventing a microcomputer from running away and from being damaged even when an

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interrupt handling or exception handling is requested during on-board programming of the above program memory (Iwata, col. 3, lines 31-34).

The combination of Yamada/Iwata does not expressly disclose a second address range corresponding to the second storage area (the second storage area being nonvolatile).

The Computer Dictionary discloses a non-volatile storage area (pg. 367, right column, paragraph 7).

The combination of Yamada/Iwata and the Computer Dictionary are analogous art because they are from the same field of endeavor, that being computer memory systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Iwata's vector address storage area B-V on Computer Dictionary's non-volatile storage area, thus providing a second address range corresponding to the second storage area.

The motivation for doing so would have been to not lose data when power is removed from the memory device (pg. 367, right column, paragraph 7), thus decreasing the power consumption needed for data retention and also increasing system reliability during power loss.

Therefore, it would have been obvious to combine Yamada, Iwata, and the Computer Dictionary for the benefit of obtaining the invention as specified in claim 15.

9. **As per claim 16**, the combination of Yamada/Iwata/The Computer Dictionary discloses the conversion circuit performs address conversion individually for a plurality

of address ranges, each of the plurality of address ranges including each of the interrupt vectors (Iwata, col. 11, lines 34-38).

10. **As per claim 17**, the combination of Yamada/Iwata/The Computer Dictionary discloses the conversion circuit comprises hardware that performs a predetermined conversion operation (Iwata, col. 11, line 65 – col. 12, line 21; Fig. 3).

11. **As per claim 19**, the combination of Yamada/Iwata/The Computer Dictionary discloses the nonvolatile memory, the central processing unit, the flag, and the conversion circuit are integrated on a same semiconductor chip (Iwata, col. 6, lines 46-50; Fig. 1, element 30).

12. **As per claim 20**, the combination of Yamada/Iwata/The Computer Dictionary discloses the interrupt program is stored in the first storage area, the interrupt vector indicates a start address of the interrupt program, the alternate interrupt program that is executed instead of the interrupt program is stored in the second storage area, and the alternate interrupt vector indicates a start address of the alternate interrupt program (Yamada, col. 8, lines 14-29; Fig. 1, element 1). *It should be noted that it is inherently required an interrupt vector store the starting address of it's corresponding interrupt handler routine (interrupt program).*

13. **As per claim 21**, the combination of Yamada/Iwata/The Computer Dictionary discloses the interrupt program is stored in the second storage area, and the interrupt vector and the alternate interrupt vector store a start address of the interrupt program (Iwata, col. 17, lines 50-58; col. 17, line 66 – col. 18, line 3; Fig. 1, element 13). *It should be noted that "built-in RAM" is analogous to "second storage area", "NMI*

handling routine RB" is analogous to "interrupt program", "vector address NMIA" is analogous to "interrupt vector", and "vector address NMIB" is analogous to "alternate interrupt vector." It should also be noted that when in user program mode or boot mode both NMIA and NMIB, which are stored in the built-in RAM, access NMI handling routine RB.

14. **As per claim 22**, the combination of Yamada/Iwata/The Computer Dictionary discloses a main program is stored in the first storage area (Iwata, col. 9, lines 8-9; Fig. 1, element 18). *It should be noted that "built-in ROM" is analogous to "first storage area."*

15. **As per claim 23**, the combination of Yamada/Iwata/The Computer Dictionary discloses a main program is stored in the first storage area (Iwata, col. 9, lines 8-9; Fig. 1, element 18).

16. **As per claim 24**, the combination of Yamada/Iwata/The Computer Dictionary discloses a main program is stored in the second storage area (Iwata, col. 10, lines 15-17; Fig. 1, element 13).

17. **As per claim 29**, Yamada discloses a microcomputer comprising:

a nonvolatile memory including at least a first storage area and a second storage area in which delete and write of data is electrically performed independently (col. 3, lines 12-19; Fig. 1, element 1); *See citation note for the similar limitation in claim 15 above.*

a central processing unit that has a mechanism to access the nonvolatile memory (col. 3, lines 19-23 and 28-29; Fig. 1, element 2).

Yamada does not expressly disclose a flag indicating that the first storage area is not accessible;

and a conversion circuit that, based on a state of the flag, converts an address indicating a storage place of an interrupt vector that is accessed by the central processing unit into an address indicating a storage place of a corresponding alternate interrupt vector.

Iwata discloses a flag indicating that the first storage area is not accessible (col. 9, lines 51-55 and 58-61; col. 10, lines 50-58; Fig. 1, element 18); *See the citation note for the similar limitation in claim 15 above.*

and a conversion circuit that, based on a state of the flag, converts an address indicating a nonvolatile storage place of an interrupt vector that is accessed by the central processing unit into an address indicating a storage place of a corresponding alternate interrupt vector (col. 14, lines 6-15; Fig. 5).

Yamada and Iwata are analogous because they are from the same field of endeavor, that being microcomputers.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Iwata's conversion circuit within Yamada's microcomputer.

The motivation for doing so would have been to improve the safety of a system during on-board programming of a program memory (Iwata, col. 3, lines 25-27). Also, another motivation for doing so would have been to provide additional safety by preventing a microcomputer from running away and from being damaged even when an

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interrupt handling or exception handling is requested during on-board programming of the above program memory (Iwata, col. 3, lines 31-34).

The combination of Yamada/Iwata does not expressly disclose an address indicating a nonvolatile storage place of a corresponding alternate interrupt vector.

The Computer Dictionary discloses a non-volatile storage area (pg. 367, right column, paragraph 7).

The combination of Yamada/Iwata and the Computer Dictionary are analogous art because they are from the same field of endeavor, that being computer memory systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Iwata's vector address storage area B-V on Computer Dictionary's non-volatile storage area, thus providing an address indicating a nonvolatile storage place of a corresponding alternate interrupt vector.

The motivation for doing so would have been to not lose data when power is removed from the memory device (pg. 367, right column, paragraph 7), thus decreasing the power consumption needed for data retention and also increasing system reliability during power loss.

Therefore, it would have been obvious to combine Yamada, Iwata, and the Computer Dictionary for the benefit of obtaining the invention as specified in claim 29.

18. Claims 1, 4, and 6-12 are rejected under 35 U.S.C. 103(a) as being obvious over Yamada in view of Iwata, Hashimoto (U.S. Patent 6,654,839), and The Computer Dictionary.

19. **As per claim 1**, Yamada discloses a microcomputer comprising:

a nonvolatile memory including at least a first storage area and a second storage area in which delete and write of data is electrically performed independently (col. 3, lines 12-19; Fig. 1, element 1); *See citation note for the similar limitation in claim 15 above.*

wherein a plurality of interrupt vectors indicating respective storage places of a plurality of interrupt programs executed upon requesting of an interrupt is stored in the first storage area (col. 8, lines 25-29; Fig. 8, elements (31-1)~(31-n));

and a plurality of alternate interrupt vectors corresponding to the respective interrupt vectors is stored in the second storage area (col. 8, lines 22-25; Fig. 8, elements (30-1)~(30-n));

a central processing unit that has a mechanism to access the nonvolatile memory (col. 3, lines 19-23 and 28-29; Fig. 1, element 2).

Yamada does not expressly disclose a flag indicating that the first storage area is not accessible;

and a conversion circuit that includes a plurality of registers to which a plurality of addresses indicating respective storage places of the alternate interrupt vectors are set, and that, based on a state of the flag, converts a first address indicating a storage place of the interrupt vector that is accessed by the central processing unit into a second address indicating a storage place of the corresponding alternate interrupt vector by outputting the second address from one of the registers corresponding to the first address.

Iwata discloses a flag indicating that the first storage area is not accessible (col. 9, lines 51-55 and 58-61; col. 10, lines 50-58; Fig. 1, element 18); *See the citation note for the similar limitation in claim 1 above.*

and a conversion circuit that includes a plurality of registers, based on a state of the flag, converts a first address indicating a nonvolatile storage place of the interrupt vector that is accessed by the central processing unit into a second address indicating a storage place of the corresponding alternate interrupt vector (col. 14, lines 6-15; col. 23, lines 60-63; Fig. 5; Fig. 19).

Yamada and Iwata are analogous because they are from the same field of endeavor, that being microcomputers.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Iwata's conversion circuit within Yamada's microcomputer.

The motivation for doing so would have been to improve the safety of a system during on-board programming of a program memory (Iwata, col. 3, lines 25-27). Also, another motivation for doing so would have been to provide additional safety by preventing a microcomputer from running away and from being damaged even when an interrupt handling or exception handling is requested during on-board programming of the above program memory (Iwata, col. 3, lines 31-34).

The combination of Yamada/Iwata does expressly disclose a second address indicating a nonvolatile storage place of the corresponding alternate interrupt vector;

a conversion circuit that includes a plurality of registers to which a plurality of addresses indicating respective storage places of the alternate interrupt vectors are set,

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and that, based on a state of the flag, converts a first address indicating a storage place of the interrupt vector that is accessed by the central processing unit into a second address indicating a storage place of the corresponding alternate interrupt vector by outputting the second address from one of the registers corresponding to the first address.

Hashimoto discloses a plurality of registers to which a plurality of addresses indicating respective storage places of the alternate interrupt vectors are set, that outputs the second address from one of the registers corresponding to the first address (col. 6, lines 41-45, 53-59, and 63-65; Fig. 5, elements 50, 54, and the "VTA (vector table address)"). *It should be noted that the "base register" and the "interrupt factor register" are analogous to the "plurality of registers."*

The combination of Yamada/Iwata and Hashimoto are analogous because they are from the same field of endeavor, that being microcomputers.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Hashimoto's registers within Yamada/Iwata's microcomputer.

The motivation for doing so would have been to make the device more convenient to the user, by enabling the storage of a series of interrupt vectors at addresses within a memory as desired by the user (Hashimoto, col. 3, lines 4-6).

The combination of Yamada/Iwata/Hashimoto does not expressly disclose a second address indicating a nonvolatile storage place of the corresponding alternate interrupt vector.

The Computer Dictionary discloses a non-volatile storage area (pg. 367, right column, paragraph 7).

The combination of Yamada/Iwata/Hashimoto and the Computer Dictionary are analogous art because they are from the same field of endeavor, that being computer memory systems:

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Iwata's vector address storage area B-V on Computer Dictionary's non-volatile storage area, thus providing a second address indicating a nonvolatile storage place of the corresponding alternate interrupt vector.

The motivation for doing so would have been to not lose data when power is removed from the memory device (pg. 367, right column, paragraph 7), thus decreasing the power consumption needed for data retention and also increasing system reliability during power loss.

Therefore, it would have been obvious to combine Yamada, Iwata, Hashimoto, and the Computer Dictionary for the benefit of obtaining the invention as specified in claim 1.

20. **As per claim 4**, the combination of Yamada/Iwata/Hashimoto/The Computer Dictionary discloses the conversion circuit comprises hardware that performs a predetermined conversion operation (Iwata, col. 14, lines 19-35; Fig. 5).

21. **As per claim 6**, the combination of Yamada/Iwata/Hashimoto/The Computer Dictionary discloses the nonvolatile memory, the central processing unit, the flag, and

the interrupt vector address conversion circuit are integrated on a same semiconductor chip (Iwata, col. 6, lines 46-50; Fig. 1, element 30).

22. **As per claim 7**, the combination of Yamada/Iwata/Hashimoto/The Computer Dictionary discloses the interrupt program is stored in the first storage area, the interrupt vector indicates a start address of the interrupt program, the alternate interrupt program that is executed instead of the interrupt program is stored in the second storage area, and the alternate interrupt vector indicates a start address of the alternate interrupt program (Yamada, col. 8, lines 14-29; Fig. 1, element 1). *See the citation note for claim 20 above.*

23. **As per claim 8**, the combination of Yamada/Iwata/Hashimoto/The Computer Dictionary discloses the interrupt program is stored in the second storage area, and the interrupt vector and the alternate interrupt vector indicate a start address of the interrupt program (Iwata, col. 17, lines 50-58; col. 17, line 66 – col. 18, line 3; Fig. 1, element 13). *See the citation note for claim 21 above.*

24. **As per claim 9**, the combination of Yamada/Iwata/Hashimoto/The Computer Dictionary discloses a main program is stored in the first storage area (Iwata, col. 9, lines 8-9; Fig. 1, element 18). *See the citation note for claim 22 above.*

25. **As per claim 10**, the combination of Yamada/Iwata/Hashimoto/The Computer Dictionary discloses a main program is stored in the first storage area (Iwata, col. 9, lines 8-9; Fig. 1, element 18).

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26. **As per claim 11**, the combination of Yamada/Iwata/Hashimoto/The Computer Dictionary discloses a main program is stored in the second storage area (Iwata, col. 10, lines 15-17; Fig. 1, element 13).

27. **As per claim 12**, the combination of Yamada/Iwata/Hashimoto/The Computer Dictionary discloses a main program is stored in the second storage area (Iwata, col. 10, lines 15-17; Fig. 1, element 13).

28. **Claim 28** is rejected under 35 U.S.C. 103(a) as being obvious over Yamada in view of Iwata, Yoshioka et al. (U.S. Patent 6,038,661) (hereinafter "Yoshioka"), and The Computer Dictionary.

29. **As per claim 28**, Yamada discloses a microcomputer comprising:

a nonvolatile memory including at least a first storage area and a second storage area in which delete and write of data is electrically performed independently (col. 3, lines 12-19; Fig. 1, element 1); *See citation note for the similar limitation in claim 15 above.*

wherein a plurality of interrupt vectors indicating respective storage places of a plurality of interrupt programs executed upon requesting of an interrupt is stored in the first storage area (col. 8, lines 25-29; Fig. 8, elements (31-1)~(31-n));

and a plurality of alternate interrupt vectors corresponding to the respective interrupt vectors is stored in the second storage area (col. 8, lines 22-25; Fig. 8, elements (30-1)~(30-n));

a central processing unit that has a mechanism to access the nonvolatile memory (col. 3, lines 19-23 and 28-29; Fig. 1, element 2).

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Yamada does not expressly disclose a flag indicating that the first storage area is not accessible;

and a conversion circuit that includes a register to which an offset is set, and that converts a first address indicating a storage place of the interrupt vector that is accessed by the central processing unit into a second address indicating a storage place of the corresponding alternate interrupt vector by adding the offset to the first address.

Iwata discloses a flag indicating that the first storage area is not accessible (col. 9, lines 51-55 and 58-61; col. 10, lines 50-58; Fig. 1, element 18); *See the citation note for the similar limitation in claim 1 above.*

and a conversion circuit that includes a register, and that converts a first address indicating a nonvolatile storage place of the interrupt vector that is accessed by the central processing unit into a second address indicating a storage place of the corresponding alternate interrupt vector (col. 14, lines 6-15; col. 23, line 60; Fig. 5; Fig. 19).

Yamada and Iwata are analogous because they are from the same field of endeavor, that being microcomputers.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Iwata's conversion circuit within Yamada's microcomputer.

The motivation for doing so would have been to improve the safety of a system during on-board programming of a program memory (Iwata, col. 3, lines 25-27). Also, another motivation for doing so would have been to provide additional safety by

preventing a microcomputer from running away and from being damaged even when an interrupt handling or exception handling is requested during on-board programming of the above program memory (Iwata, col. 3, lines 31-34).

The combination of Yamada/Iwata does expressly disclose a second address indicating a nonvolatile storage place of the corresponding alternate interrupt vector;

a conversion circuit that includes a register to which an offset is set, and that converts a first address indicating a storage place of the interrupt vector that is accessed by the central processing unit into a second address indicating a storage place of the corresponding alternate interrupt vector by adding the offset to the first address.

Yoshioka discloses a register to which an offset is set, that adds the offset to the first address (col. 15, lines 17-26; col. 17, lines 23-31; Fig. 14). *It should be noted that the "shifter" is a form of a shift register.*

The combination of Yamada/Iwata and Yoshioka are analogous because they are from the same field of endeavor, that being microcomputers.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Yoshioka's vector offset hardware within Yamada/Iwata's microcomputer.

The motivation for doing so would have been to make it possible to accomplish both a reduction in the physical scale of the circuit and an increase in the data processing speed (Yoshioka, col. 24, lines 60-63).

The combination of Yamada/Iwata/Yoshioka does not expressly disclose a second address indicating a nonvolatile storage place of the corresponding alternate interrupt vector.

The Computer Dictionary discloses a non-volatile storage area (pg. 367, right column, paragraph 7).

The combination of Yamada/Iwata/Yoshioka and the Computer Dictionary are analogous art because they are from the same field of endeavor, that being computer memory systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Iwata's vector address storage area B-V on Computer Dictionary's non-volatile storage area, thus providing a second address indicating a nonvolatile storage place of the corresponding alternate interrupt vector.

The motivation for doing so would have been to not lose data when power is removed from the memory device (pg. 367, right column, paragraph 7), thus decreasing the power consumption needed for data retention and also increasing system reliability during power loss.

Therefore, it would have been obvious to combine Yamada, Iwata, Yoshioka, and the Computer Dictionary for the benefit of obtaining the invention as specified in claim 28.

30. Claim 18 is rejected under 35 U.S.C. 103(a) as being obvious over Yamada in view of Iwata and The Computer Dictionary as applied to claim 15 above, and

further in view of Andrew S. Tanenbaum, Structured Computer Organization, 2nd Edition (hereinafter "Tanenbaum").

31. **As per claim 18**, the combination of Yamada/Iwata/The Computer Dictionary discloses the conversion circuit performs a predetermined conversion operation based on a setting by a hardware (Iwata, col. 14, lines 36-54; Fig. 5). *It should be noted that the conversion is performed based on the settings of the logic circuits and selection circuits (i.e. hardware).*

The combination of Yamada/Iwata/The Computer Dictionary does not expressly disclose the conversion circuit performs a predetermined conversion operation based on a setting by a software.

Tanenbaum discloses that hardware and software are logically equivalent (pg. 11, line 11).

The combination of Yamada/Iwata and Tanenbaum are analogous art because they are from the same field of endeavor, that being computer systems design.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to follow Tanenbaum's argument and base Yamada/Iwata/The Computer Dictionary's conversion operation on software settings.

The motivation for doing so would have been to optimize such factors as cost, speed, and reliability (Tanenbaum, pg. 11, lines 14-15).

Therefore, it would have been obvious to combine Yamada/Iwata/The Computer Dictionary and Tanenbaum for the benefit of obtaining the invention as specified in claim 18.

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32. Claim 5 is rejected under 35 U.S.C. 103(a) as being obvious over Yamada in view of lwata, Hashimoto, and The Computer Dictionary as applied to claim 1 above, and further in view of Tanenbaum.

33. As per claim 5, the combination of Yamada/lwata/Hashimoto/The Computer Dictionary discloses the conversion circuit performs a predetermined conversion operation based on a setting by a hardware (lwata, col. 14, lines 36-54; Fig. 5). *It should be noted that the conversion is performed based on the settings of the logic circuits and selection circuits (i.e. hardware).*

The combination of Yamada/lwata/Hashimoto/The Computer Dictionary does not expressly disclose the conversion circuit performs a predetermined conversion operation based on a setting by a software.

Tanenbaum discloses that hardware and software are logically equivalent (pg. 11, line 11).

The combination of Yamada/lwata/Hashimoto and Tanenbaum are analogous art because they are from the same field of endeavor, that being computer systems design.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to follow Tanenbaum's argument and base Yamada/lwata/Hashimoto/The Computer Dictionary's conversion operation on software settings.

The motivation for doing so would have been to optimize such factors as cost, speed, and reliability (Tanenbaum, pg. 11, lines 14-15).

Therefore, it would have been obvious to combine Yamada/Iwata/Hashimoto/The Computer Dictionary and Tanenbaum for the benefit of obtaining the invention as specified in claim 5.

34. Claims 26-27 are rejected under 35 U.S.C. 103(a) as being obvious over Yamada in view of Iwata and The Computer Dictionary as applied to claims 20-21, and further in view of Fudeyasu et al. (U.S. Patent 6,154,837).

35. As per claims 26-27, the combination of Yamada/Iwata/The Computer Dictionary discloses all the limitations of claims 26-27 except a main program is stored in a memory other than the nonvolatile memory.

Fudeyasu discloses a main program is stored in a memory other than the nonvolatile memory (col. 3, lines 37-41; col. 4, lines 25-28; Fig. 1, elements 2 and 4). *It should be noted that "boot ROM" is analogous to "nonvolatile memory."*

The combination of Yamada/Iwata/The Computer Dictionary and Fudeyasu are analogous art because they are from the same field of endeavor, that being interrupt processing within microcomputers.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Fudeyasu's RAM within Yamada/Iwata/The Computer Dictionary's microcomputer.

The motivation for doing so would have been to offer the advantage of being able to provide a microcomputer that can achieve effective interrupt processing in boot mode by enabling an erase/write program to execute interrupt processing freely (Fudeyasu, col. 5, lines 5-9).

Therefore, it would have been obvious to combine Yamada/Iwata/The Computer Dictionary and Fudeyasu for the benefit of obtaining the inventions as specified in claims 26-27.

36. Claims 13-14 are rejected under 35 U.S.C. 103(a) as being obvious over Yamada in view of Iwata, Hashimoto, and The Computer Dictionary as applied to claims 7-8, and further in view of Fudeyasu.

37. As per claims 13-14, the combination of Yamada/Iwata/Hashimoto/The Computer Dictionary discloses all the limitations of claims 13-14 except a main program is stored in a memory other than the nonvolatile memory.

Fudeyasu discloses a main program is stored in a memory other than the nonvolatile memory (col. 3, lines 37-41; col. 4, lines 25-28; Fig. 1, elements 2 and 4).
See citation note for claims 26-27 above.

The combination of Yamada/Iwata/Hashimoto/The Computer Dictionary discloses and Fudeyasu are analogous art because they are from the same field of endeavor, that being interrupt processing within microcomputers.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Fudeyasu's RAM within Yamada/Iwata/Hashimoto/The Computer Dictionary discloses's microcomputer.

The motivation for doing so would have been to offer the advantage of being able to provide a microcomputer that can achieve effective interrupt processing in boot mode by enabling an erase/write program to execute interrupt processing freely (Fudeyasu, col. 5, lines 5-9).

Therefore, it would have been obvious to combine Yamada/Iwata/Hashimoto/The Computer Dictionary discloses and Fudeyasu for the benefit of obtaining the inventions as specified in claims 13-14.

Response to Arguments

38. Applicant's arguments filed in the communication dated April 19, 2007 with respect to **claims 1 and 4-27** have been fully considered but they are not persuasive.

39. With respect to Applicant's argument in the second full paragraph under section I of the communication filed October 31, 2007, the Examiner respectfully disagrees. The Examiner is interpreting the combination of both Iwata's address conversion circuit (Fig. 5) and control circuit (FCONT) as disclosing Applicant's conversion circuit. Thus, in this configuration Iwata does in fact disclose a conversion circuit that includes a first and second pair of registers. Also, as discussed by Applicant themselves, registers PEREG, MBREG1, and MBREG2 are used to program the flash memory. Thus, PEREG and MBREG1 is capable of setting a first address range corresponding to a first storage area and PEREG and MBREG2 is capable of setting a second address range corresponding to a second storage range. Accordingly, the combination of Yamada and Iwata sufficiently discloses a conversion circuit that includes a first pair of registers for setting a first address range corresponding to the first storage area and a second pair of registers for setting a second address range corresponding to the second storage area.

40. With respect to Applicant's argument in the third full paragraph under section I of the communication filed October 31, 2007, the Examiner respectfully disagrees. The

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Examiner submits that the Computer Dictionary is clearly in the field of computer memory systems because the Computer Dictionary describes, in great detail, the state of various aspects of the art at the time of its publication. The entry of non-volatile memory within the Computer Dictionary not only serves as a mere definition, but more importantly as a clear disclosure that non-volatile memory was well known in the art at the time of the Computer Dictionary's publication. Also, the motivation provided by the Examiner as to why one would add non-volatile memory to an invention is extremely well known throughout the art. Thus, the disclosure of non-volatile memory in the Computer Dictionary in combination with Yamada and Iwata sufficiently discloses the invention as claimed in claim 15.

41. With respect to Applicant's arguments in the sixth full paragraph of the communication filed October 31, 2007, Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references. The Examiner refers Applicant to the rejection of claim 29 above.

42. With respect to Applicant's arguments in the eighth full paragraph of the communication filed October 31, 2007, Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references. The Examiner refers Applicant to the rejection of claim 1 above.

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43. With respect to Applicant's arguments in the eleventh full paragraph of the communication filed October 31, 2007, Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references. The Examiner refers Applicant to the rejection of claim 28 above.

44. As for Applicant's arguments with respect to the dependent claims, the arguments rely on the allegation that the independent claims are allowable and therefore for the same reasons the dependent claims are allowable. However, as addressed above, the independent claims are not allowable, thus, Applicant's arguments with respect to the dependent claims are not persuasive.

Conclusion

STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by MPEP 707.70(i):

CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, **claims 1 and 4-29** have received a second action on the merits and are subject of a second action final.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

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A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arpan P. Savla whose telephone number is (571) 272-1077. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on (571) 272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



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